

REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-16 are in the case. Claims 1-6, 8, 10-13, 15 and 16 have been amended. The Specification has been amended.

Applicants acknowledge with appreciation the indication of allowability of Claims 8-10, 13 and 14 if re-written to overcome the 35 U.S.C. 112, 2nd paragraph rejection(s). Applicants have so re-written those claims, as described below, and so their allowance is respectfully requested.

Applicants acknowledge with appreciation the indication of allowability of Claims 3-5 if re-written to overcome the 35 U.S.C. 112, 2nd paragraph rejection(s) and to include all of the limitations of the base and any intervening claims. Applicants have re-written those claims to overcome the 35 U.S.C. 112, 2nd paragraph rejection(s). However, in view of the arguments set forth below, applicants respectfully decline at this time to re-write these claims to make them independent.

Regarding the objection to the Specification, paragraph [0039] has been amended to correct the noted informality. Applicants note that the sentence to which objection was made is now in conformity with the rest of the Specification, for example lines 1-4 of paragraph [0036]. It is respectfully submitted that the objection has been overcome, wherefore its reconsideration and withdrawal are respectfully requested.

Regarding the rejection of Claims 1-16 under 35 U.S.C. 112, 2nd paragraph, the term "complementary" has been eliminated from all claims, and "first and second bias transistors" has been changed in all instances to "third and fourth bias transistors" to maintain consistency. It is therefore respectfully submitted that this ground for rejection has been overcome.

Regarding the allegation that the use of the terms "first and second source/drain regions of the switching transistor" is indefinite, this ground of rejection is respectfully traversed. Applicants note that this terminology is consistent with the Specification, for example in lines 6 and 8 of paragraph

[0031], lines 2 and 6 of paragraph [0032], etc. It is respectfully submitted that this terminology is clear, and is utilized because the switching transistor is typically symmetrical as between source and drain, and so ascribing the term “source” or “drain” to one or the other is arbitrary and potentially unnecessarily limiting of the scope of the claims. In addition, it is respectfully submitted that in accordance with such usage Figure 3 shows that the switching transistor 14 has two source/drain regions, one connected to capacitor 12_A and the other to capacitor 12_B.

Regarding the allegation that in Claim 3 that the first and second bias transistors, now the third and fourth bias transistors, cannot be on at the same time as the switching transistor, this ground of rejection is respectfully traversed. Applicants respectfully point out that the third and fourth bias transistors read on transistors 16_A and 16_B of Figure 3. It is the first and second bias transistors (previously, first and second complementary bias transistors) that read on transistors 18_A and 18_B of Figure 3. Note that the third and fourth transistors are recited as being connected to “a reference voltage”, while the first and second transistors are connected to “a bias voltage”. The “reference voltage” reads on the voltage at ground in Figure 3, while the “bias voltage” reads on the bias voltage V_P .

Regarding the alleged indefiniteness of the phrase “strong reverse bias” in Claims 6 and 15, both of these claims have been amended to clarify that this reverse bias is of the source/drain regions *with respect to an underlying substrate or well, as the case may be*. Support for this is found in lines 1-4, and et seq., of paragraph [0036] of the Specification. It is therefore respectfully submitted that this ground for rejection has been overcome.

It is therefore respectfully submitted that all claims are now clear and definite. Wherefore reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 1, 6, 15 and 16 under 35 U.S.C. § 102(b) as allegedly being anticipated by Okata, this rejection is respectfully traversed. Claim 1 recites a switched variable capacitor including a switching field-effect

transistor, a first capacitor and a second capacitor, as well as first and second bias transistors having a conduction path connected between a bias voltage and the first and second source/drain regions of the switching transistor, respectively, and having a gate coupled to the gate of the switching transistor, so that the first and second complementary bias transistors are turned on when the switching transistor is turned off. The recited first and second bias transistors so connected provide the benefit of allowing the parasitic junction capacitance at the junction of the source/drain regions of the switching transistor and its underlying substrate or well, as the case may be, to be minimized, thereby allowing a larger maximum-to-minimum capacitance ratio of the variable capacitor.

The patent to Otaka apparently relates to attenuation circuitry in which a gate current controls the conduction of FETs in order to vary attenuation. As such, it is respectfully submitted that Otaka is non-analogous art. There is no disclosure or suggestion of any variable capacitor. Otaka is concerned with providing a variable attenuator in which the ON-state resistance of an FET used as a gain control switch, such as transistor Q21 in his Figure 6, depends less on the input signal. Significantly, in Otaka's Figure 6 his transistors Q22 and Q23 are not connected to a bias voltage as required in Claim 1. Rather, they are connected to an A.C. ground which, as shown in his Figure 5, is simply a capacitor connected to ground. Thus, there is no biasing of the source/drain regions of his transistor Q21 by transistors Q22 and Q23. Instead, they merely provide a path to ground for the AC signals, through resistors R22 and R23, respectively, so as to form the π -type attenuator structure shown in his Figure 7 when they are turned on. In addition, Otaka's bias setting circuit, for example bias setting circuit 23 in his Figure 6, is not switched, as are the first and second bias transistors in Claim 1, and is intended to control the ON-state voltage between the gate and source/drain of his transistor Q21 in order to maintain a more constant ON-state resistance as the input signal varies. In Claim 1, the first and second bias transistors are turned on when the switching transistor is turned off to minimize parasitic capacitance during the OFF state of the switching

transistor, so as to allow a larger maximum-to-minimum capacitance ratio of the variable capacitor, a different mechanism for a different purpose. Otaka does mention parasitic capacitance, because he is concerned with parasitic capacitance between his Q21's source/drain region and gate, as it causes pass-through of his signal in attenuation mode, and thereby reduces the effective attenuation. However, he reduces this parasitic capacitance by reducing the gate width of his Q21 (by implication from his Q11; see column 5, lines 11-39).

Therefore, it is respectfully submitted that the patent to Otaka neither shows nor suggests the invention as recited in Claim 1. The other art of record is even less relevant. Claim 15 has similar limitations to those in Claim 1 discussed above, and so the above reasons apply as well to Claim 15. It is respectfully submitted that for those reasons Claims 1 and 15 are allowable over Otaka and, indeed, over all of the art of record whether considered individually or in any combination. Claim 6 depends from Claim 1 and Claim 16 depends from Claim 15, and so those claims are allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claim 2 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Okata, this rejection is respectfully traversed. Claim 2 depends from Claim 1. The reasons for the allowability of Claim 1 over Okata are set forth above and apply as well to Claim 2, and so it is respectfully submitted that Claim 2 is allowable for those reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claim 7 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Okata in view of Paul, this rejection is respectfully traversed. Claim 7 depends from Claim 1. The reasons for the allowability of Claim 1 over Okata are set forth above and apply as well to Claim 7. The patent to Paul fails to cure the deficiencies of Okata, it having been cited merely to show capacitors being of the metal-to-metal type. Accordingly, it is respectfully

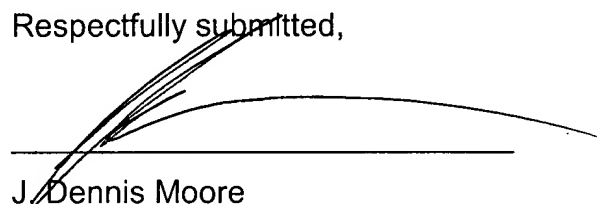
submitted that Claim 7 is allowable. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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